Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A rate limiting circuit for enabling an enable line to a unit for transferring data, comprising:

a register storing a rate limiting parameter value;

a clock generator generating a clock signal having a frequency related to the rate limiting parameter value;

a counter incremented by the clock signal; and

a controller enabling the enable line to the unit if a count of the counter is greater than zero so that a data transmission rate associated with the unit is not greater than the frequency of the clock signal.

2. (original) The rate limiting circuit according to claim 1, wherein if the count of the counter is not greater than zero at the time of receiving a request to access the unit, the controller waits until the count is greater than zero before enabling the enable line.

3. (original) The rate limiting circuit according to claim 1, wherein the controller decrements the counter by a count of one each time it enables the enable line.

4. (original) The rate limiting circuit according to claim 1, wherein the register is electrically programmable.

5. (original) The rate limiting circuit according to claim 4, wherein the register is electrically erasable.

6. (original) The rate limiting circuit according to claim 1, wherein the register is programmed by a metal mask pattern during fabrication of the rate limiting circuit.

7. (original) The rate limiting circuit according to claim 1, wherein the unit for transferring data is a buffer.

8. (original) The rate limiting circuit according to claim 7, wherein the enable line is a read enable line used to read contents of the buffer.

9. (original) The rate limiting circuit according to claim 7, wherein the enable line is a write enable line used to write data into the buffer.

10. (original) The rate limiting circuit according to claim 1, wherein the unit for transferring data is a DMA controller.

11. (original) The rate limiting circuit according to claim 1, wherein the controller reads the rate limiting parameter value from the register and provides it to the clock generator so that the clock generator generates the clock signal having the frequency related to the rate limiting parameter value.

12. (original) The rate limiting circuit according to claim 11, wherein the clock generator generates the clock signal from an input clock signal, and the frequency of the clock signal generated by the clock generator is equal to the reciprocal of a product of the period of the input clock signal times the sum of one plus the rate limiting parameter value.

13. (original) The rate limiting circuit according to claim 1, further comprising a second register storing a second rate limiting parameter value, wherein the frequency of the clock signal generated by the clock generator is related to the larger of the rate limiting parameter value and the second rate limiting parameter value.

14. (original) The rate limiting circuit according to claim 13, wherein the second register is a one-time programmable memory.

15. (original) The rate limiting circuit according to claim 13, wherein the rate limiting circuit is included in an integrated circuit device and the second register is programmed during manufacture of the integrated circuit device.

16. (original) The rate limiting circuit according to claim 15, wherein the second register is programmed by a metal mask pattern during fabrication of the integrated circuit device.

17. (original) The rate limiting circuit according to claim 13, wherein the controller reads the rate limiting parameter value from the register and the second rate limiting parameter value from the second register, and provides the larger of rate limiting parameter value and the second rate limiting parameter value to the clock generator so that the clock generator generates the clock signal having the frequency related to the larger of the rate limiting parameter value and the second rate limiting parameter value.

18. (original) The rate limiting circuit according to claim 17, wherein the clock generator generates the clock signal from an input clock signal, and the frequency of the clock signal generated by the clock generator is equal to the reciprocal of a product of the period of the input clock signal times the sum of one plus the larger of the rate limiting parameter value and the second rate limiting parameter value.

19. (original) A rate limiting circuit for enabling an enable line to a unit for transferring data, comprising:

a data storage unit storing a rate limiting parameter value; and

logic coupled to the data storage unit and an input clock signal such that the logic enables the enable line at a rate between successive such enabling that is no greater than a maximum frequency equal to the reciprocal of a product of the period of the input clock signal times the sum of one plus the rate limiting parameter value.

20. (original) The rate limiting circuit according to claim 19, wherein the data storage unit is electrically programmable.

21. (original) The rate limiting circuit according to claim 19, wherein the data storage unit is electrically erasable.

22. (original) The rate limiting circuit according to claim 19, wherein the data storage unit is programmed by a metal mask pattern during manufacture of the rate limiting circuit.

23. (original) The rate limiting circuit according to claim 19, wherein the unit for transferring data is a buffer.

24. (original) The rate limiting circuit according to claim 23, wherein the enable line is a read enable line used to read contents of the buffer.

25. (original) The rate limiting circuit according to claim 23, wherein the enable line is a write enable line used to write data into the buffer.

26. (original) A rate limiting circuit for enabling an enable line to a unit for transferring data, comprising:

a first data storage unit storing a first rate limiting parameter value;

a second data storage unit storing a second rate limiting parameter value; and

logic coupled to the first data storage unit, the second data storage unit, and an input clock signal such that the logic enables the enable line at a rate between successive such enabling that is no greater than a maximum frequency equal to the reciprocal of a product of the period of the input clock signal times the sum of one plus the larger of the first and the second rate limiting parameter values.

27. (original) The rate limiting circuit according to claim 26, wherein the first data storage unit is electrically erasable and electrically programmable, and the second data storage unit is one-time programmable memory programmed during manufacture of a device including the rate limiting circuit.

28. (original) The rate limiting circuit according to claim 26, wherein the unit for transferring data is a buffer.

29. (original) The rate limiting circuit according to claim 28, wherein the enable line is a read enable line used to read contents of the buffer.

30. (original) The rate limiting circuit according to claim 28, wherein the enable line is a write enable line used to write data into the buffer.

31. (original) A rate limiting circuit for enabling an enable line to a unit for transferring data, comprising:

a first data storage unit storing a first rate limiting parameter value programmed by a user of the rate limiting circuit;

a second data storage unit storing a second rate limiting parameter value programmed by a manufacturer of the rate limiting circuit; and

logic coupled to the first and the second data storage units so as to enable the enable line at a rate between successive such enabling that is no greater than a maximum frequency determined from the larger of the first and the second rate limiting parameter values.

32. (original) The rate limiting circuit according to claim 31, wherein the first data storage unit is electrically erasable and electrically programmable, and the second data storage unit is an one-time programmable memory programmed during manufacture of a device including the rate limiting circuit.

33. (original) The rate limiting circuit according to claim 31, wherein the unit for transferring data is a buffer.

34. (original) The rate limiting circuit according to claim 33, wherein the enable line is a read enable line used to read contents of the buffer.

35. (original) The rate limiting circuit according to claim 33, wherein the enable line is a write enable line used to write data into the buffer.

36. (canceled).

37. (currently amended) A method for enabling an enable line to a unit for transferring data, comprising:

reading a rate limiting parameter value from a register;

~~The method according to claim 36, further comprising~~ receiving an input clock signal characterized by a period; and

enabling the enable line at a rate between successive such enabling that is no greater than a maximum frequency determined from the rate limiting parameter value, wherein the maximum frequency is equal to the reciprocal of the product of the period of the input clock signal times the sum of one plus the rate limiting parameter.

38. (original) The method according to claim 37, further comprising reading a second rate limiting parameter value from a second register, wherein the maximum frequency is equal to the reciprocal of the product of the period of the input clock signal times the sum of one plus the larger of the rate limiting parameter value and the second rate limiting parameter value.

39. (original) The method according to claim 38, further comprising writing the rate limiting parameter value into the register.

40. (original) The method according to claim 39, further comprising programming the second rate limiting parameter value into the second register on a one-time-programmable basis.

41. (original) The method according to claim 40, wherein the programming of the second rate limiting parameter value is performed during the manufacture of a device including the second register.

42. (original) A method for enabling an enable line to a unit for transferring data, comprising:

reading a first rate limiting parameter value from a first register;

reading a second rate limiting parameter value from a second register; and

enabling the enable line at a rate between successive such enabling that is no greater than a maximum frequency determined from the larger of the first rate limiting parameter value and the second rate limiting parameter value.